FPIX - Electronics

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Director's Review

November 1, 2002

Response to Recommendation 1 TBM

DMILL chip has been fully tested:

- works completely as designed at full 40 MHz
  - → 6 Tested / 5 Fully Functional
- power consumption 600 mW
  - → core 140 mW
  - → LVDS driver 460 mW

Translation to 0.25 micron started:

- follow PSI schedule for ROC
  - → 1st submission Feb. ’03
  - → 2nd “final” submission Oct. ’03
  - → delivery of “final” chip end of ’03

Response to Recommendation 1 TBM

Resources:

- Ed Bartz full time on TBM for next 12 months

  Exception: Ed will work on FEC between submission and delivery of 1st prototype

Concerns:

- coupling of submission schedule to PSI

  → commits to 5-layer IBM process via CERN

  → if 3rd submission needed must be engineering run

  CERN multiproject submissions are 3-layers

  3rd submission could be part of production !

Response to Recommendation 2 — System Tests

DMILL Plaquette (1x5, 2x5) without sensors

FEC (Version 1) / DMILL TBM / VHDI (DMILL) / PSI43 ROC

developments needed: None

⇒ end of ‘02

DMILL Plaquette (1x5, 2x5) with sensors

FEC (Version 1) / DMILL TBM / VHDI (DMILL) / PSI43 ROC

developments needed: bump bonded sensors

⇒ Spring of ‘02

0.25 μm Plaquette

FEC (Version 2) / PGA TBM / VHDI (0.25 μm) / 0.25 μm ROC

developments needed: 0.25 μm ROC, VHDI (0.25 μm)

⇒ Fall of ‘03

Response to Recommendation 2 — System Tests

Panel (one side of blade)

FEC (Version 2) / HDI / 0.25 μm TBM / VHDI / ROC

developments needed: HDI / 0.25 μm TBM

⇒ end of '03

Blade

FEC (Version 3) / HDI / TBM / VHDI / ROC / FED

developments needed: FEC (version 3) / FED

⇒ Summer of '04

Multiple (3) Blades

FEC (Version 3) / HDI / TBM / VHDI / ROC / Port Card

developments needed: Port Card

⇒ End of '04

Response to Recommendation 3 — Port Card

Problems with Port Card at Detector:

- not enough space for opto-hybrids
- opto-hybrids introduce extra connectors

Possible solution:

- mount optical components directly of Port Card

  $\rightarrow$ large engineering effort

  (not enough resources)

$\Rightarrow$ Move Port Card to Service Cylinder

Response to Recommendation 3 — Port Card

Disadvantages:

- need up to 50 cm pigtail
- need control link splitter

} needed for barrel anyway

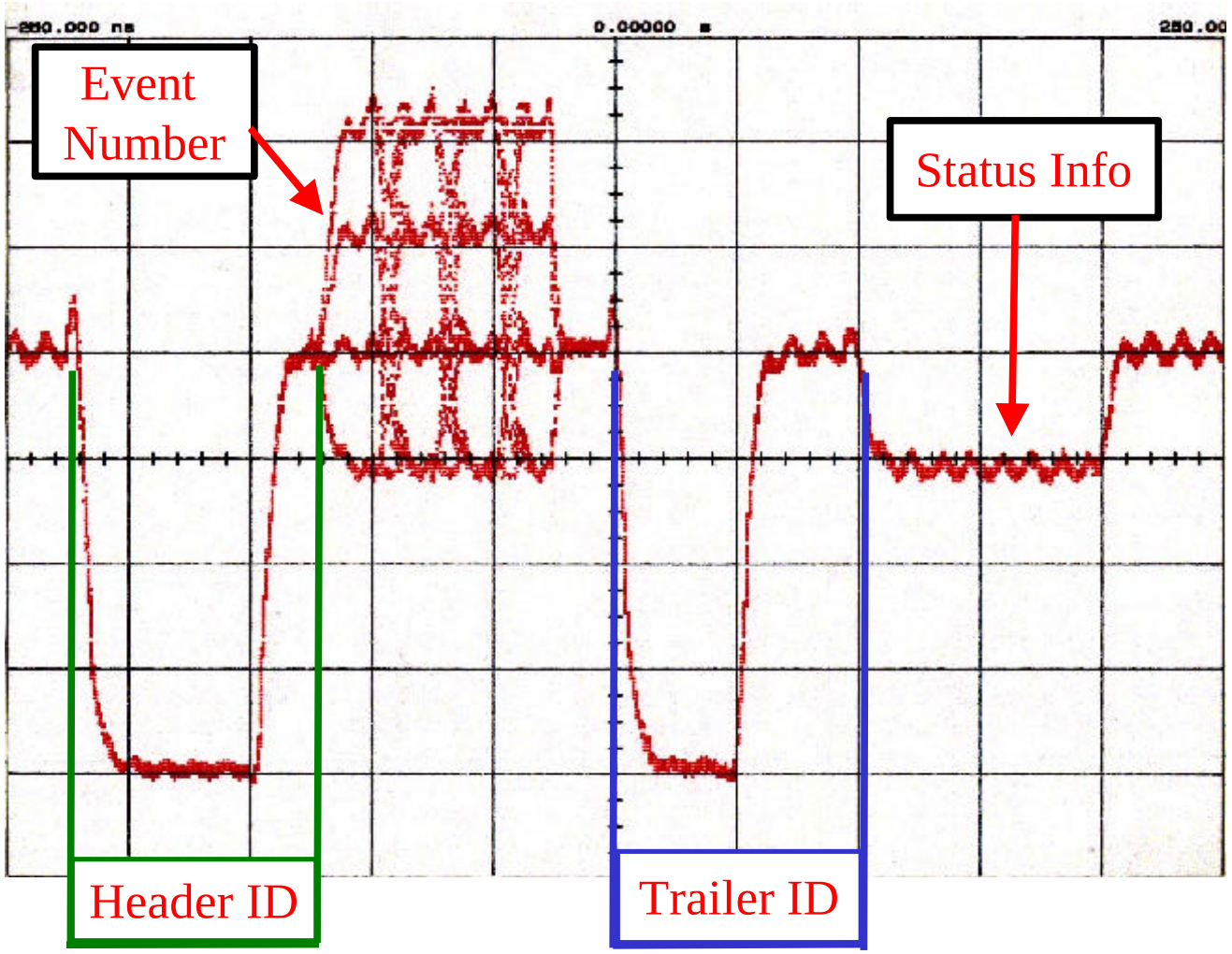
Advantages:

- more space for port card
- material moved out to larger η
- opens up option for 6 blades per link

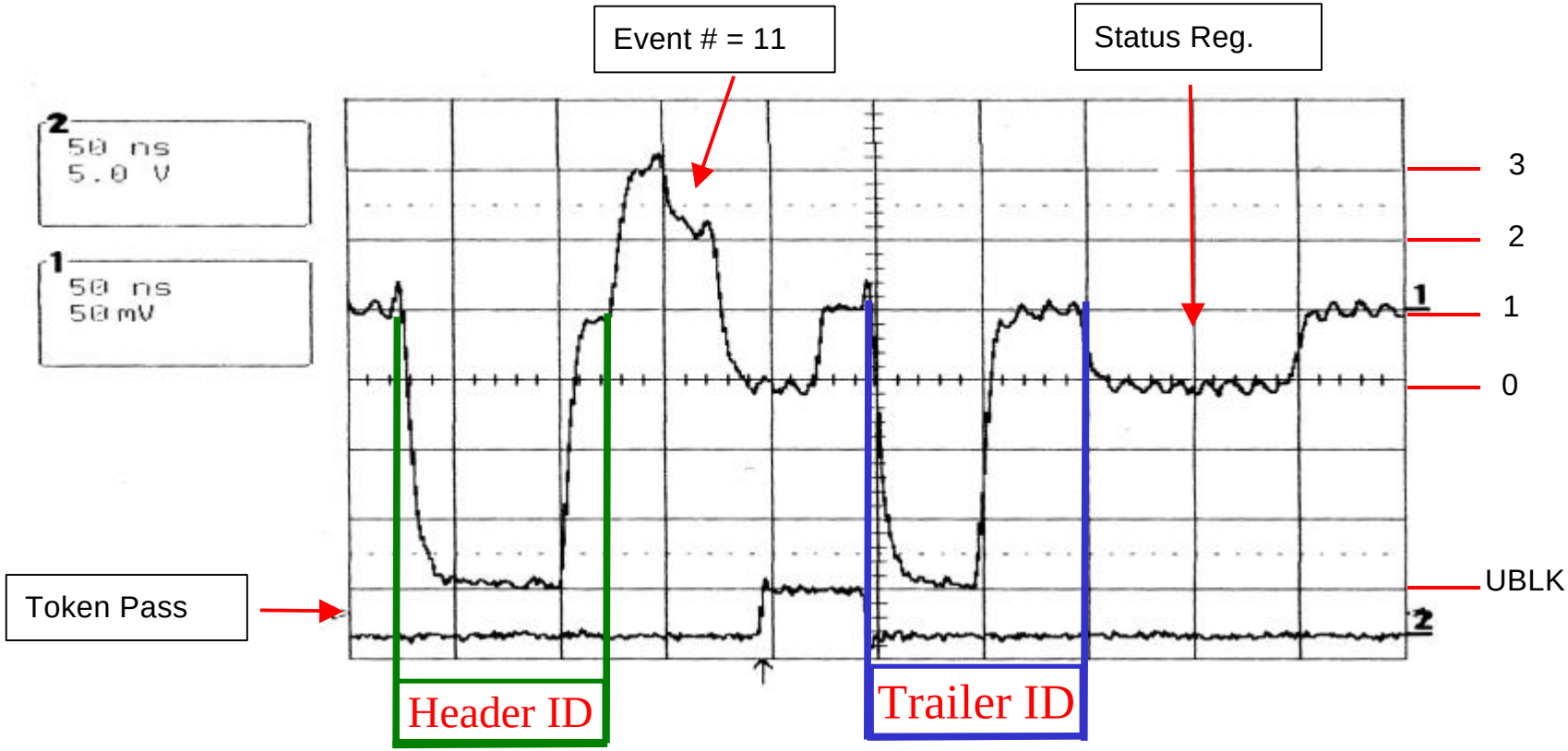
Slides 9 – 16
are Supplemental

1 MHz Trigger Rate

Expected Max CMS Trigger Rate = 100KHz



TBM Test Results



- Header marker 3 “UBLK” + “1”
  - –8 Bit Event Number (4 Clocks)
- Trailer marker 2 “UBLK” + 2 “1”
  - –8 Bit Status Word (4 Clocks)

Analog Level Discrimination

Level Separation:

- UBlk ↔ Level_0 550 Cts
- Adjacent Levels 215 Cts

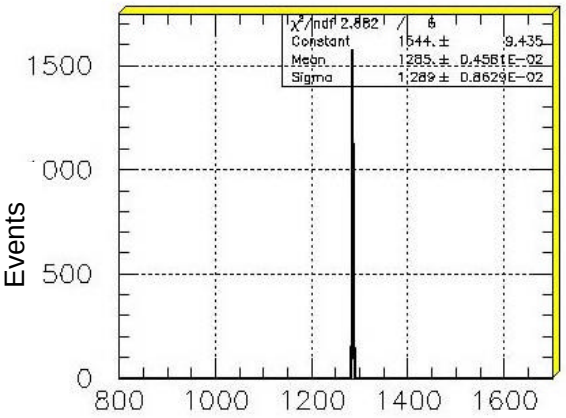
•Noise:

- Ublk **s** = 1.29 Cts
- Level **s** = 2.78 Cts

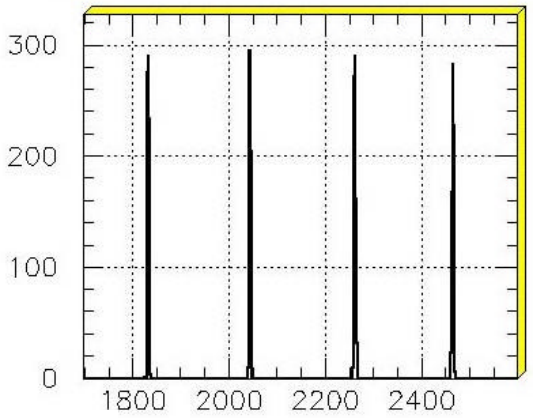
$$\frac{\sigma}{\text{Level Sep.}} = 1.3\ \%$$

(Based on 5000 Headers)

UBLK

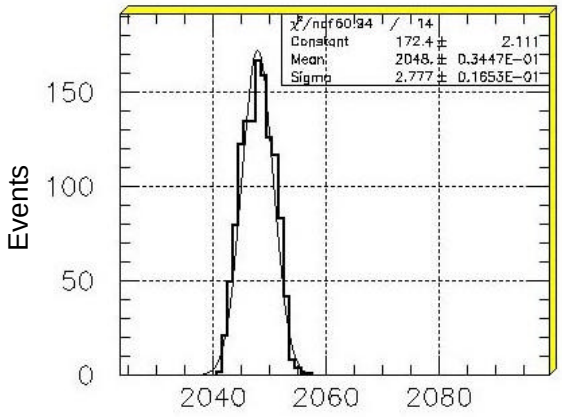


L0 L1 L2 L3

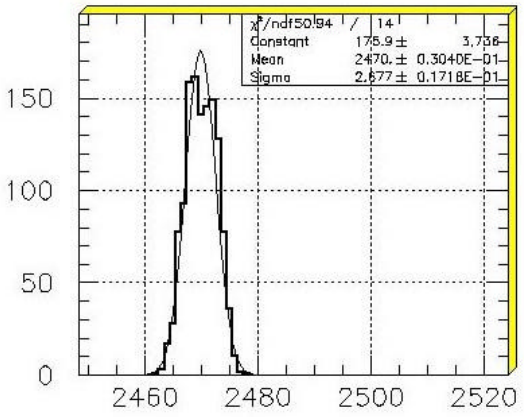


ADC Counts

L1 Expanded

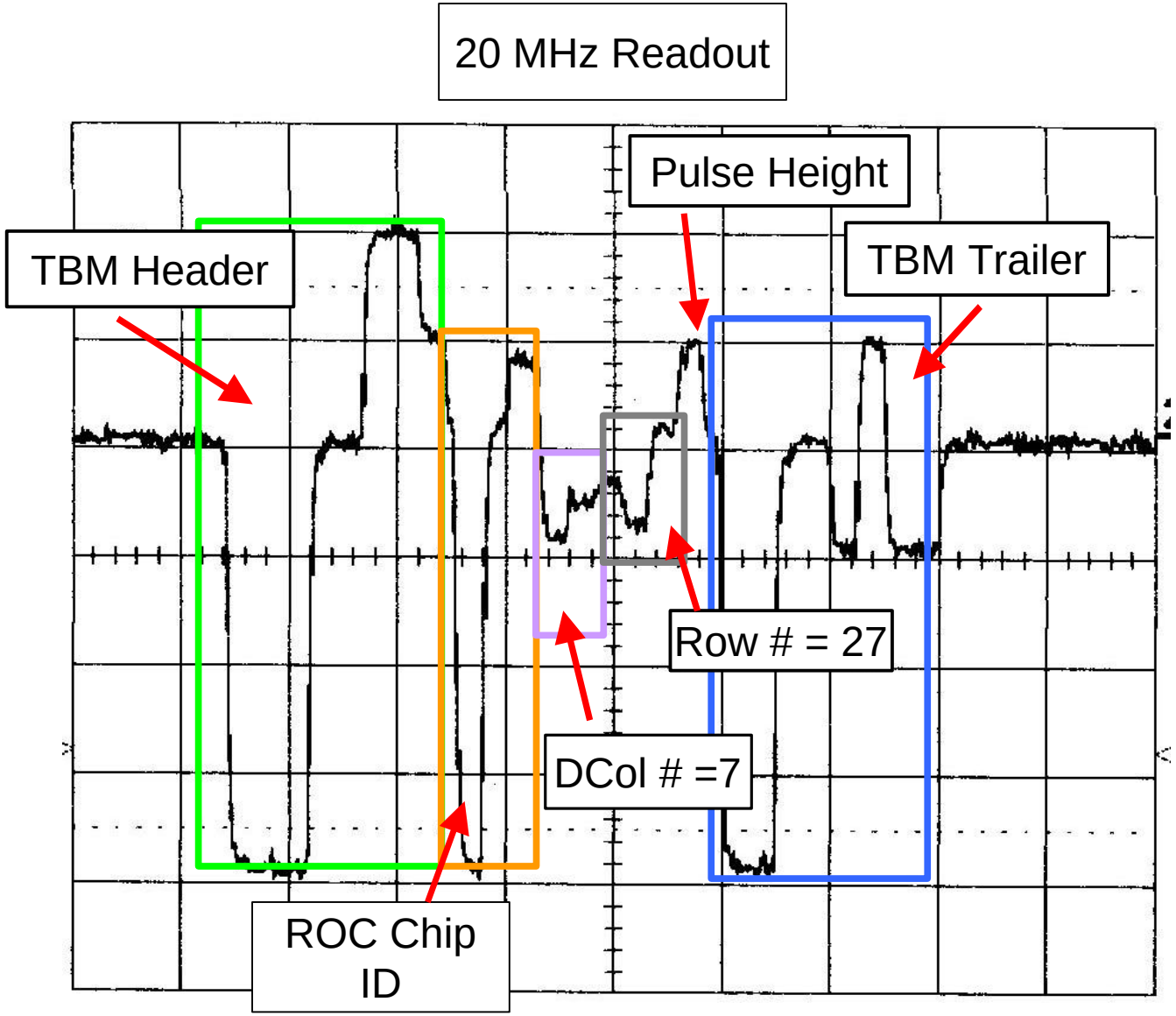


L3 Expanded



ADC Counts

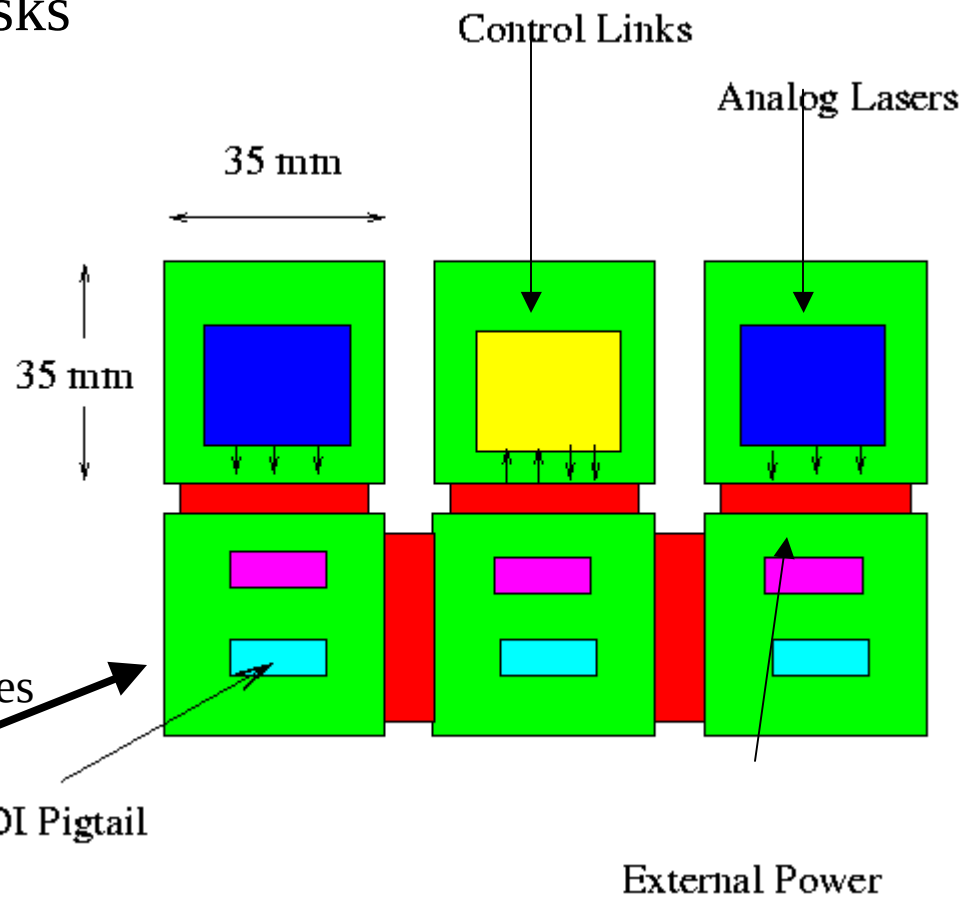
Single Pixel Calibration Pulse



Old Port Card Concept

- Multi-layer board
- Located at outer radius of disks
- 1 Port Card for 3 blades

  (8 Port Cards / disk)
- Distributes power to blades
- Houses
  - lasers and laser driver chips
    - 6 analog lasers
    - 1 control network laser
  - photodiodes and receiver chips
    - 2 control network photodiodes



Port Card concept

- folds around cooling fin
  - green → rigid
  - red → flex

Opto-Hybrids

CERN Digital and Analog Optical Hybrids

⇒ include connector pads

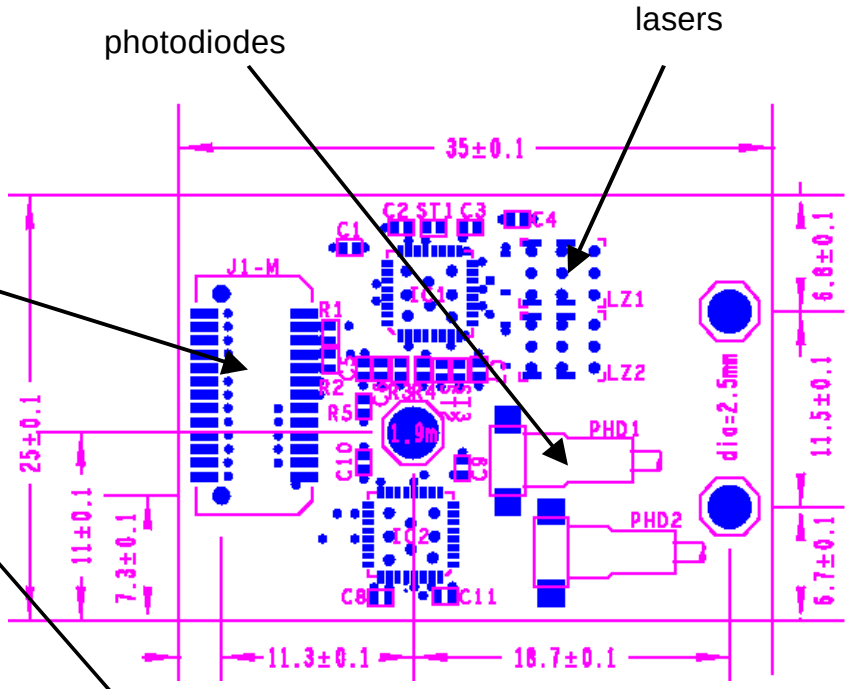
→ wasteful in space and material

⇒ Prefer to mount components

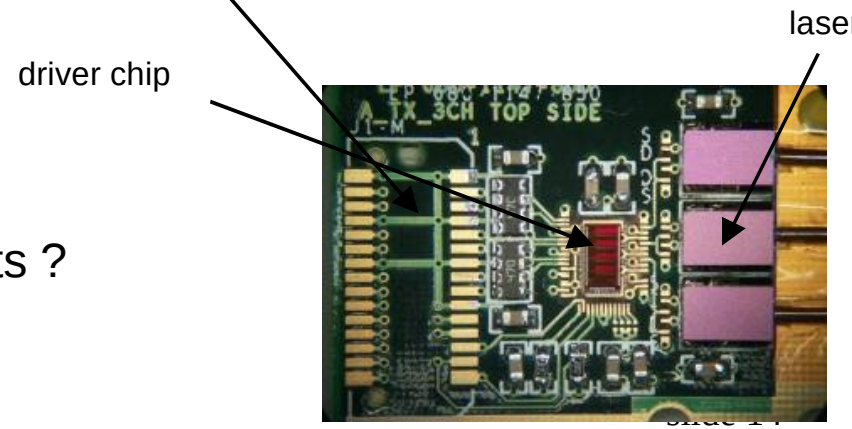
- lasers
- driver chip
- photodiodes
- receiver chip
- surface mount comp.

directly onto Port Card

Can we get individual components ?

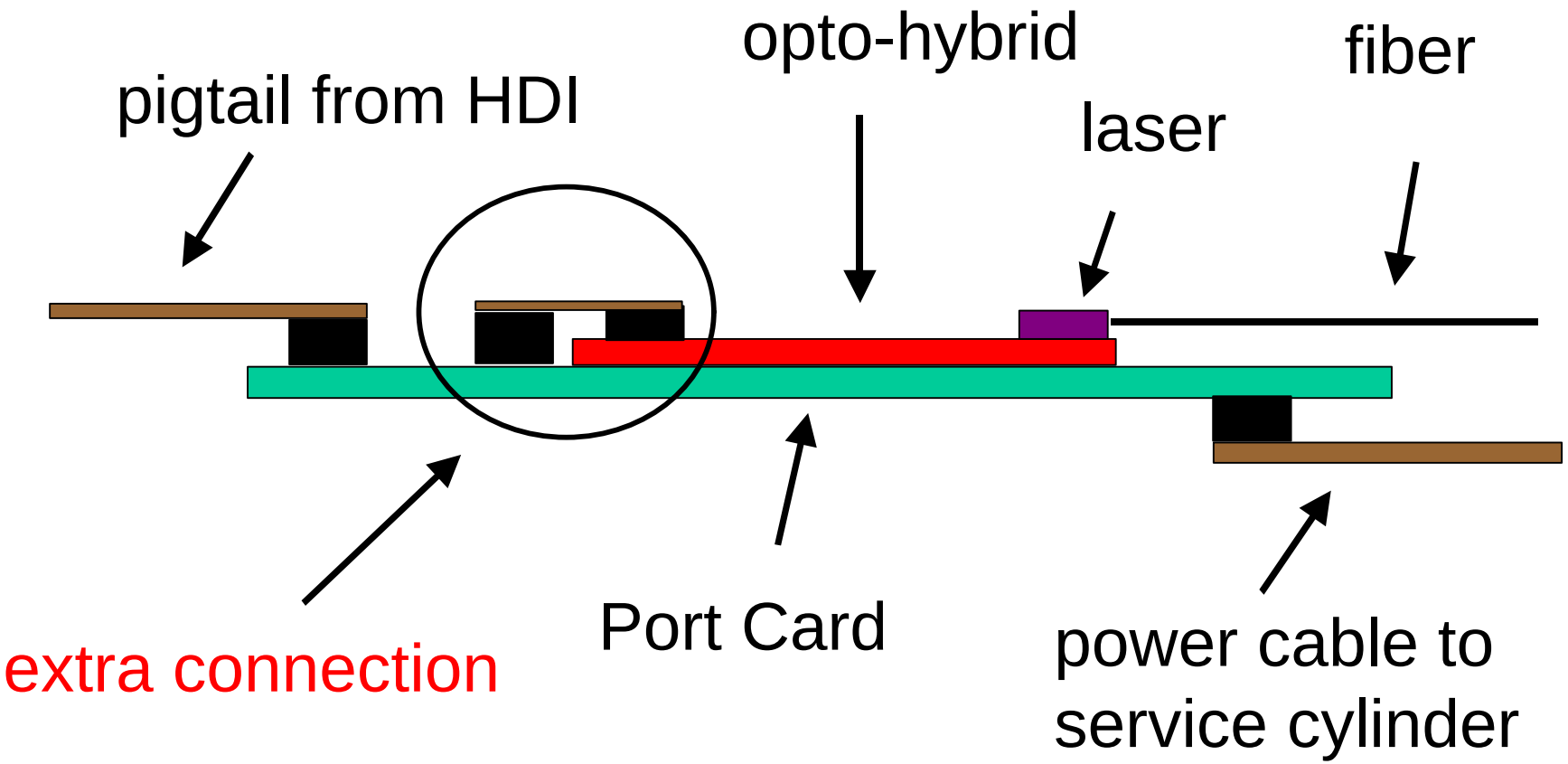


Digital hybrid



Analog hybrid

Port Card using CERN Opto-hybrid



Port Card with Components Individually Mounted